What is Claimed is:

[c1] A device adapted to function as an antifuse, said device comprising a first conductor, a second conductor, and an insulator between said first and second conductors, said device having first discrete regions having a first programming voltage and second discrete regions having a second programming voltage less than said first programming voltage.

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[c2] The invention of claim 1 wherein said second discrete regions are increased in area by providing at least one of said conductors with a plurality of fingers separated by a plurality of gaps, said second discrete regions comprising at least a portion of an edge of said fingers.

[c3] The invention of claim 1 wherein said first conductor comprises a gate material and said second conductor comprises a doped area bounded by shallow trench isolation.

[c4] The invention of claim 1 wherein said first conductor is substantially orthogonal to said second conductor.

[c5] The invention of claim 4 wherein each of said plurality of fingers have a finger width, and wherein said second discrete regions are increased in area by decreasing said finger width and by forming an increased number of said fingers on said at least one conductor.

[c6] The invention of claim 1 wherein a programming event comprises a substantially vertical current path between said first conductor and said second conductor.

[c7] The invention of claim 6 wherein said programming event comprises the application of a voltage between said first conductor and said second conductor, said voltage substantially equal to the minimum voltage sufficient to create said current path.

[c8] The invention of claim 7 wherein said minimum voltage is substantially equal to a burn-in voltage for said device.

[c9] An antifuse on a chip comprising a dielectric material positioned between a conductor and an active area, said dielectric material having a first thickness, wherein discrete portions of said dielectric material have a second thickness less than said first thickness where an edge portion of one of said conductor and said active area overlaps the other of said conductor and said active area.

[c10] The invention of claim 9 wherein one of said conductor and said active area comprise a plurality of fingers having a width substantially equal to a minimum feature size.

[c11] The invention of claim 10 wherein said plurality of fingers are formed in said conductor, said fingers overlying a first portion of said active area, spaces between said plurality of fingers exposing a second portion of said active area, said first portion of said active area comprising a non-highly doped region and said second portion of said active area comprising a highly-doped region.

[c12] The invention of claim 11 wherein said highly-doped region and said non-highly doped region comprise an N-type implant.

[c13] The invention of claim 9 wherein a short between said conductor and said active area through one or more of said discrete portions of said dielectric material programs said antifuse.

[c14] The invention of claim 13 wherein said short is induced by application of a voltage from an on-chip voltage source to one of said conductor and said active area.

[c15] A method for increasing the statistical programming of an antifuse, said method comprising the steps of:
forming a first conductor and a second conductor separated by a dielectric material; and
increasing an intersection perimeter of said antifuse.

[c16] The method of claim 15 wherein said step of increasing an intersection perimeter of said antifuse comprises the step of forming a plurality of fingers in at least one of said conductors by patterning and etching, said fingers separated by a plurality of gaps.

[c17] The method of claim 16 wherein said step of forming a plurality of fingers comprises forming a plurality of regions of thin perimeter oxide.

[c18] The method of claim 15 further comprising the step of decreasing post-program resistance of said antifuse.

[c19] The method of claim 18 wherein said step of decreasing post-program resistance comprises the step of increasing the conductivity of portions of at least one of said first conductor and said second conductor that form a current path when said antifuse is

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programmed.

[c20] The method of claim 16 wherein said plurality of fingers are patterned using a process selected from the group consisting of edge printing, printing with dual tone resist, and sidewall image transfer.

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